subsequent 15 sectors is executed so as to complete the horizontal error correction for one block. If no error is detected from all sectors, the error correcting operation is complete; if there is an error detected even from one sector, the next process including vertical error correction will be executed.

As described hereinbefore, in the present embodiment, data are transferred from the buffer memory 4 not only to the syndrome calculator 5 but also to the error detector 7 at the same time, and until an error-containing code is detected by the syndrome calculator 5, error detection in the error detector 7 is executed concurrently with syndrome calculation. In the error detection performed after the error correction of the error corrector 6, the mid-term results of the error detection before the detection of the error-containing code transmitted to and stored in the mid-term result register 8 are used. This eliminates the need for all data to be transferred from the buffer memory 4 to the error detector 7. In addition, the error detecting process can start at a halfway point. Hence, the time required for error correction can be greatly reduced.

To be more specific, when the error rate is 0.05%, 2048-byte main data contain one error on the average, which means that the error is likely to arise around the central code word on the average of 12 code words in the horizontal direction. Therefore, the mid-term results register 8 has the first 6 code words, and only the remaining 6 code words can be transferred after error correction. Thus, the time required for error detection is also reduced approximately in half.

(Embodiment 2)

The present embodiment differs from the prior art in that the

syndrome calculator 5 provides the system control unit 1 with an error-containing code sector detection signal 22, which indicates that an error-containing code word has been detected from the sector.

Figure 7 shows the structure of the error correction device of the present embodiment.

The behavior of the error correction device of the present embodiment will be described as follows with reference to the procedure of horizontal error correction in one sector shown in Figure 8.

Step (c-1): the same process as at step (b-1) in Embodiment 1 is performed.

Step (c-2): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (c-3): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 to the buffer memory 4. The bus control unit 3 then outputs the syndrome data supply signal 15 and the error detector data supply signal 20 to the syndrome calculator 5 and the error detector 7, respectively, so as to supply the data read from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7 (same as at step (b-3) in the first embodiment).

Step (c-4): the syndrome calculator 5 performs error-containing-code detection every transferred code word, and outputs the syndrome 16 to the error corrector 6. When an error-containing code word is detected in one sector, the syndrome calculator 5 outputs the error-containing code sector detection signal 22 to the system control unit 1. On the other hand, the

error detector 7 also executes an error detecting process for the data transferred.

Step (c-5): the same process as at step (a-5) of the prior art is performed.

Step (c-6): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read data therefrom. Then, the bus control unit 3 outputs the error corrector access signal 18 to the error corrector 6 to supply the data read from the buffer memory 4 thereto.

Step (c-7): the same process as at step (a-7) in the prior art is performed.

Step (c-8): the same process as at step (b-8) in the first embodiment is performed.

Step (c-4) is executed in parallel with steps (c-5) through (c-8) like a pipeline.

Step (c-9): the same process as at step (a-9) in the prior art is performed.

Step (c-10): the same process as at step (a-10) in the prior art is performed.

Step (c-11): the same process as at step (b-11) in the first embodiment is performed.

Step (c-12): the same process as at step (a-12) in the prior art is performed.

When an error-containing code is not detected in one sector by the syndrome calculator 5 at step (c-4), the error correcting operations between